AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. - 13. Canceled

14. (Original) A digital adjustable chip oscillator, comprising:

a voltage control oscillator generating an oscillation signal, receiving a control voltage to adjust the frequency of the oscillation signal, and receiving an operating voltage to stabilize the frequency of the oscillation signal;

a reference voltage circuit generating a reference voltage;

a voltage regulation circuit receiving the reference voltage and generating the operating voltage; and

a digital tuning circuit receiving a digital code to adjust the control voltage and receiving the operating voltage to stabilize the control voltage.

15. (Original) The digital adjustable chip oscillator as claimed in claim 14, wherein the voltage control oscillator is a relaxation oscillator.

16. (Original) The digital adjustable chip oscillator as claimed in claim 14, wherein the reference voltage circuit is a bandgap reference voltage circuit.

17. (Original) The digital adjustable chip oscillator as claimed in claim 5, further comprising a prescaler receiving the oscillation signal and generating a period dividing signal according to a period dividing code.

18. (Original) The digital adjustable chip oscillator as claimed in claim 14, wherein the voltage regulation circuit comprises:

an operational transconductance amplifier receiving the reference voltage, receiving a loop voltage, and outputting a bias voltage;

a transistor receiving the bias voltage, outputting a current, and outputting the operating voltage; and

a loop circuit receiving the current and outputting the loop voltage.

19. Canceled.

20. (Original) The digital adjustable chip oscillator as claimed in claim 14, wherein the digital tuning circuit further comprises:

an operational transconductance amplifier receiving the reference voltage, receiving a loop voltage, and outputting the bias voltage;

a transistor receiving the bias voltage, outputting a reference current, and proportioning the bias current of the plurality of current mirrors to the reference current wherein the bias voltage is coupled to the plurality of current mirrors; and

a loop circuit receiving the reference current and outputting the loop voltage.

21. (Original) The digital adjustable chip oscillator as claimed in claim 14, wherein the digital tuning circuit further comprises:

a plurality of charge current mirrors receiving a bias voltage to generate a plurality of bias currents corresponding to the bit of the digital code and receiving the operating voltage to stabilize the plurality of bias currents;

a plurality of discharge current mirrors receiving the bias current to generate a plurality of bias currents corresponding to the bit of the digital code;

a transistor receiving the plurality of bias currents to generate the control voltage;

a plurality of first switches coupled to the plurality of current mirrors and the transistor and receiving the digital code to select the plurality of charge current mirrors; and

a plurality of second switches coupled to the plurality of current mirrors and the transistor and receiving the digital code to select the plurality of charge current mirrors.

22. (Original) The digital adjustable chip oscillator as claimed in claim 14, wherein it further comprises:

a frequency detector receiving the oscillation signal, a first reference signal with a first frequency, and a second reference signal with a second frequency, wherein when the oscillation frequency lies between the first frequency and the second frequency, the frequency detector will output a high voltage comparison signal, otherwise the frequency detector will output a low voltage comparison signal;

a programmable counter receiving a clock signal to trigger the counting and generating the digital code;

a programmable controller receiving the high voltage comparison signal to generate an enable signal directing the frequency detector to hold the high voltage comparison signal and directing the programmable counter to stop counting and hold the digital code; and

a programmable memory receiving the enable signal to record the digital code.

23. Canceled.

24. (Original) The digital adjustable chip oscillator as claimed in claim 22, wherein the programmable memory is a programmable gate writer.

25. (Original) The digital adjustable chip oscillator as claimed in claim 22, wherein the frequency detector comprises:

a first phase frequency detector receiving the first reference signal, receiving the oscillation signal, and generating a first detection signal;

a first low-pass filter receiving the first detection signal and outputting the dc component of the first detection signal;

a first comparator receiving the dc component of the first detection signal and generating a first comparison signal wherein when the first reference frequency lies above the oscillation frequency, the first comparison signal is high-level, otherwise the first comparison signal is low-level;

a second phase frequency detector receiving the second reference signal, receiving the oscillation signal, and generating a second detection signal;

a second low-pass filter receiving the second detection signal and outputting the dc component of the second detection signal;

a second comparator receiving the dc component of the second detection signal and generating a second comparison signal wherein when the second reference frequency lies above the oscillation frequency, the second comparison signal is high-level, otherwise the second comparison signal is low-level; and

an exclusive gate receiving the first comparison signal, receiving the second comparison signal, and generating the comparison signal.

26. (Original) The digital adjustable chip oscillator as claimed in claim 25, wherein the first low-pass filter and the second low-pass filter are both switch capacitance filters.

27. – 68. Canceled.